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GB 2201268 A US 4327410 A

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Online database: WPI

(54) Preserving configuration information in non-volatile memory

(57) A control information storage unit writes control information for a printer (10) in a volatile RAM (16) during normal operation. When the power source is turned off, the control information stored in the RAM is transferred to an EEPROM (17) while the supply voltage is dropping. Thus, when the power source is turned off, the control information is maintained in the EEPROM in a stable state without the need for a backup power source.

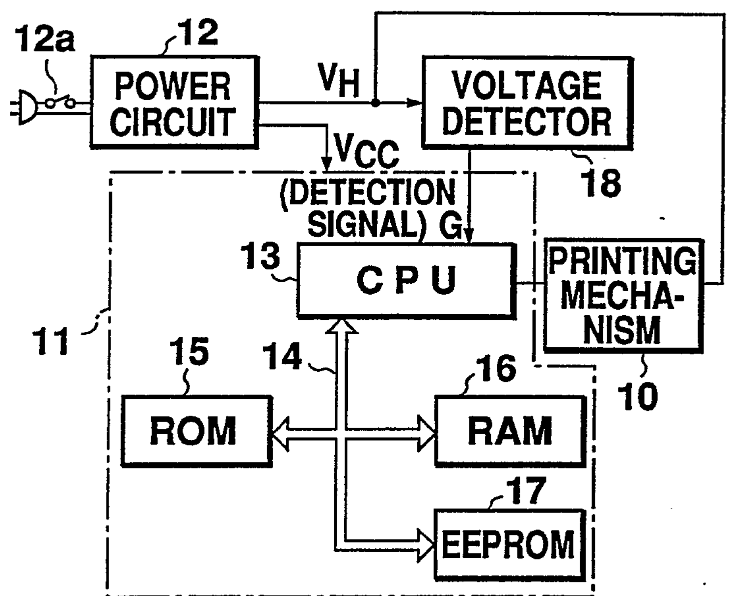


Fig. 1

GB 2 257 274 A

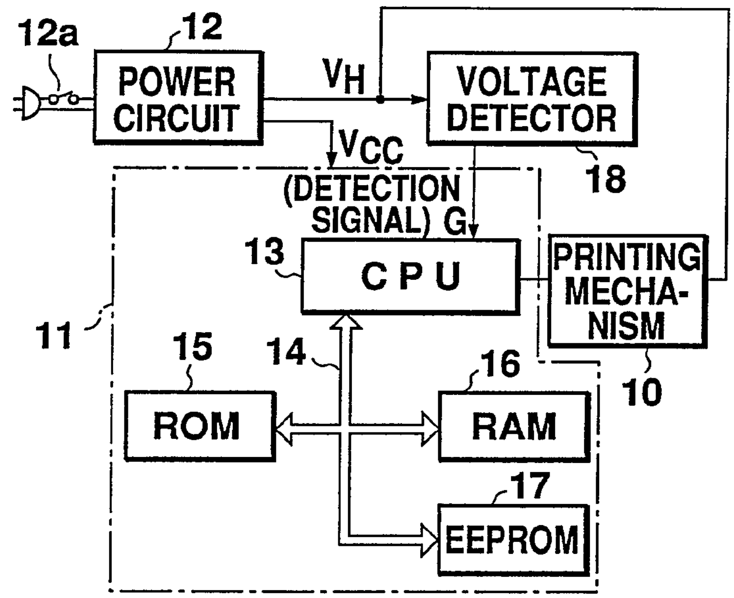

12a
12
POWER CIRCUIT
VH
VOLTAGE DETECTOR
VCC
18
(DETECTION SIGNAL) G
13
CPU
PRINTING MECHA-NISM
11
15
14
16
10
ROM
RAM
17
EEPROM

Fig. 1

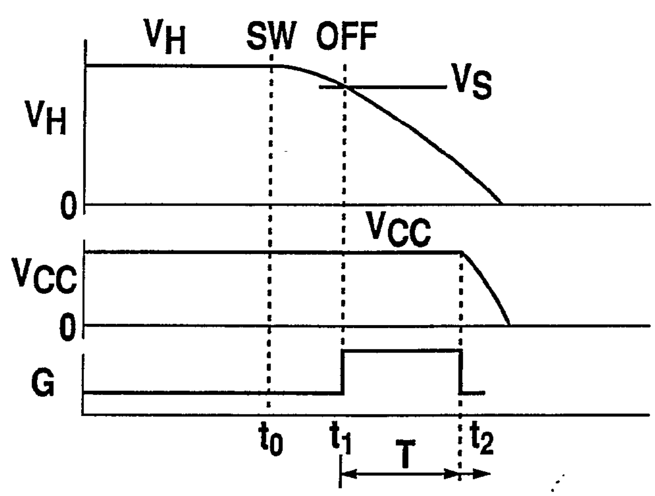

VH
SW OFF
VS
VH
0
VCC
VCC
0
G
t0
t1
T
t2

Fig. 2

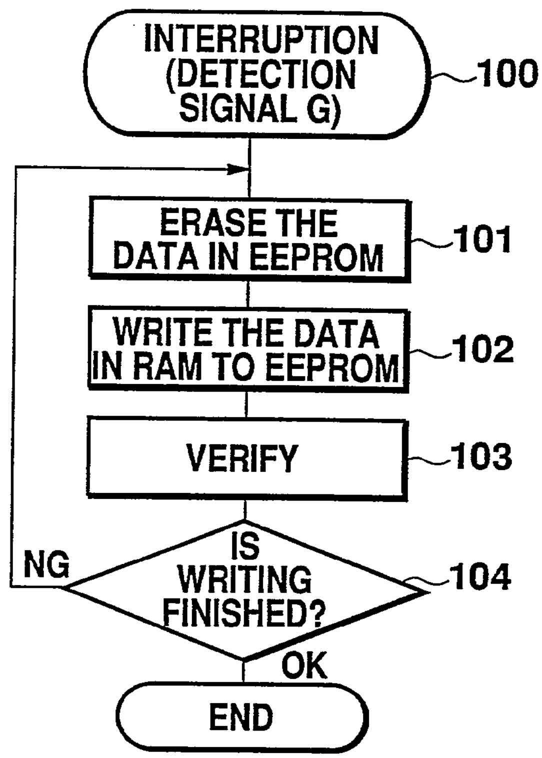

INTERRUPTION (DETECTION SIGNAL G)
100
ERASE THE DATA IN EEPROM
101
WRITE THE DATA IN RAM TO EEPROM
102
VERIFY
103
IS WRITING FINISHED?
104
NG
OK
END

Fig. 3

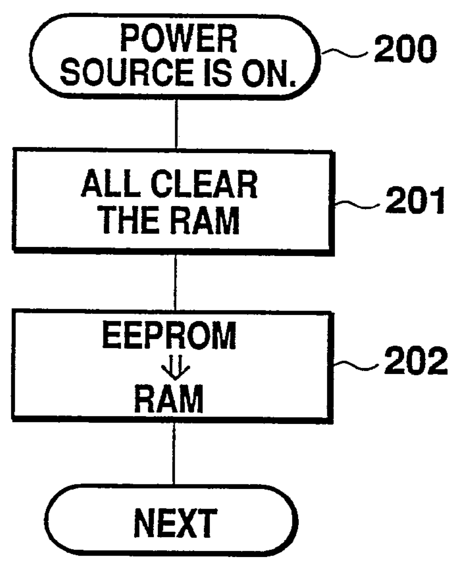

POWER SOURCE IS ON.
200
ALL CLEAR THE RAM
201
EEPROM ⇓ RAM
202
NEXT

Fig. 4

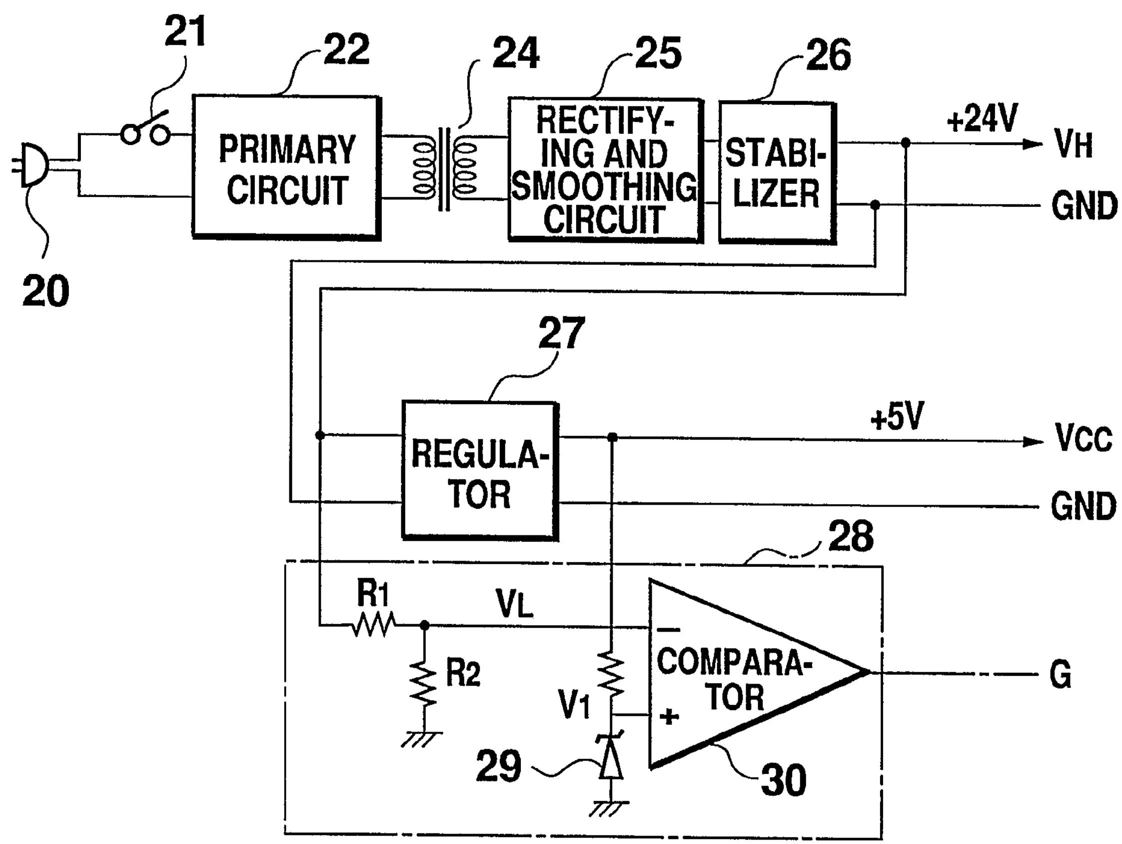

20
21
22
PRIMARY CIRCUIT
24
25
RECTIFY-ING AND SMOOTHING CIRCUIT
26
STABI-LIZER
+24V
VH
GND
27
REGULA-TOR
+5V
VCC
GND
28
R1
VL
R2
V1
29
COMPARA-TOR
30
G

Fig. 5

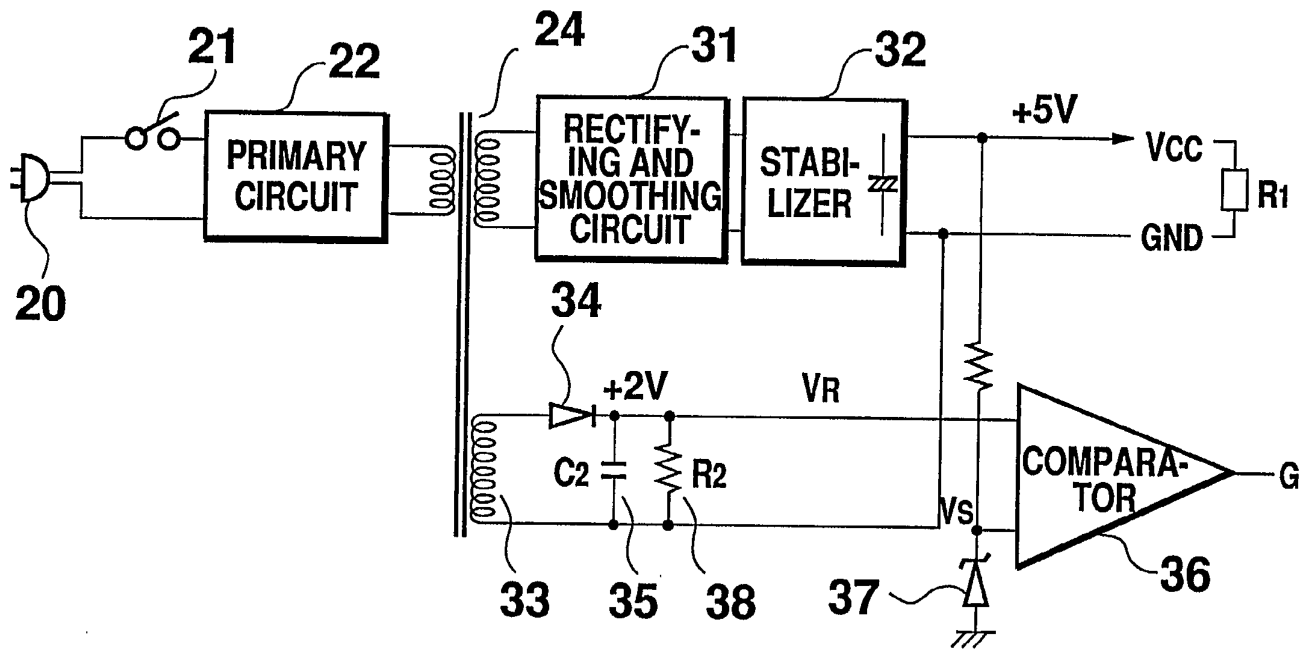

20
21
22
PRIMARY CIRCUIT
24
31
RECTIFYING AND SMOOTHING CIRCUIT
32
STABILIZER
+5V
VCC
GND
R1
34
+2V
VR
C2
R2
Vs
COMPARATOR
G
33
35
38
37
36

Fig. 6

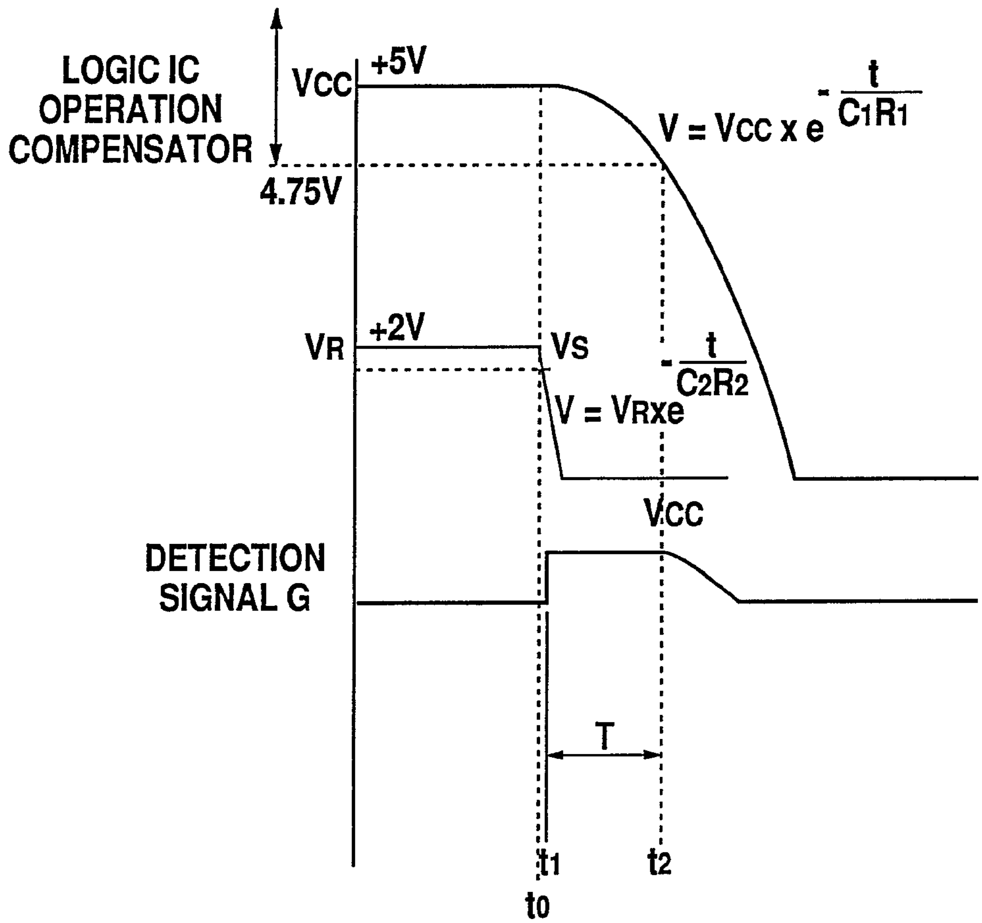

LOGIC IC
OPERATION
COMPENSATOR
Vcc
+5V
4.75V
V = Vcc x e^-t/C1R1
VR
+2V
Vs
V = VRxe^-t/C2R2
Vcc
DETECTION
SIGNAL G
T
t1
t2
t0

Fig. 7

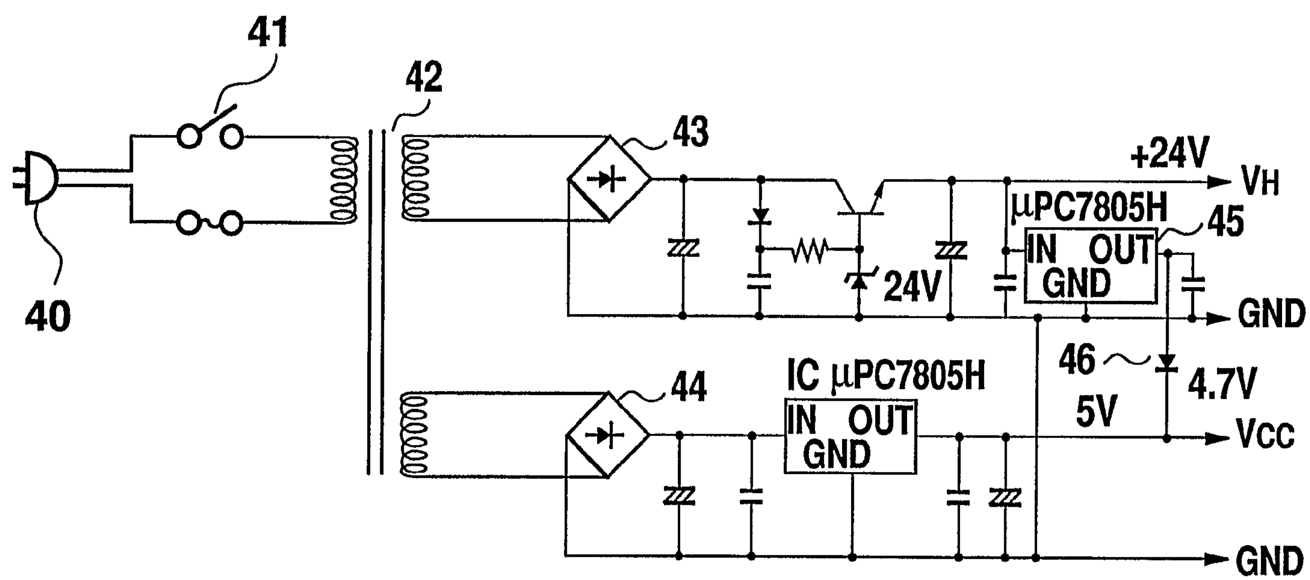
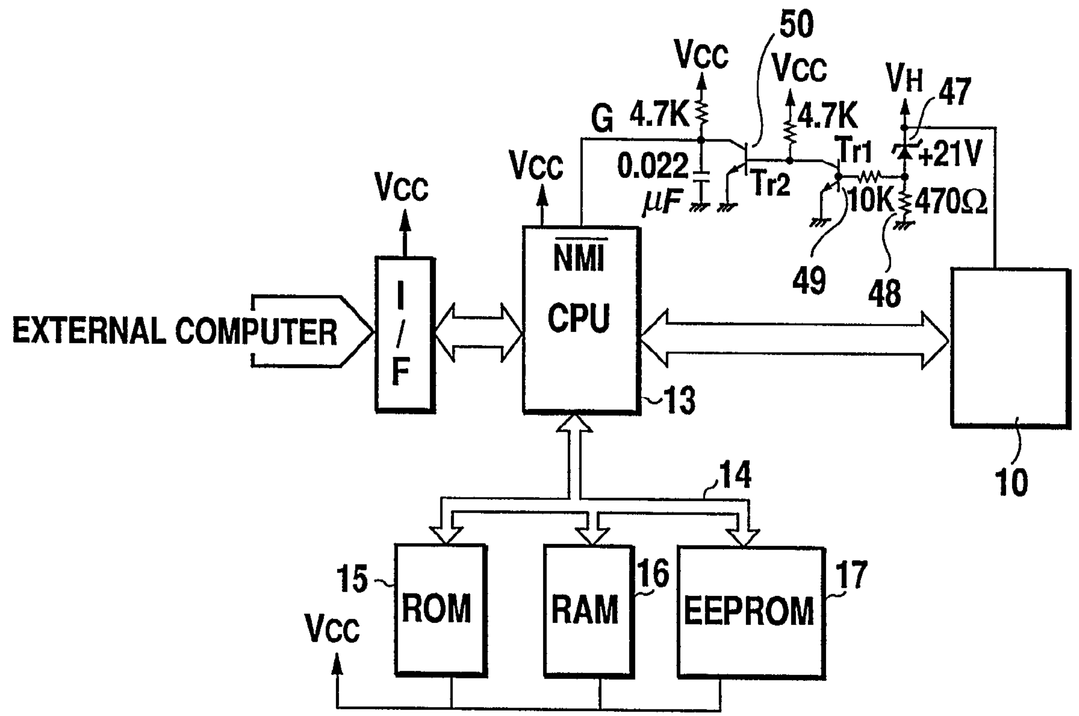

41
42
43
+24V
VH
μPC7805H
IN OUT
GND
45
24V
GND
40
46
4.7V
44
IC μPC7805H
IN OUT
GND
5V
Vcc
GND

Fig. 8



EXTERNAL COMPUTER
I / F
Vcc
NMI
CPU
13
G
4.7K
Vcc
0.022 μF
50
Tr2
4.7K
Tr1
10K
49
VH
47
+21V
470Ω
48
10
14
15
ROM
16
RAM
17
EEPROM

Fig. 9

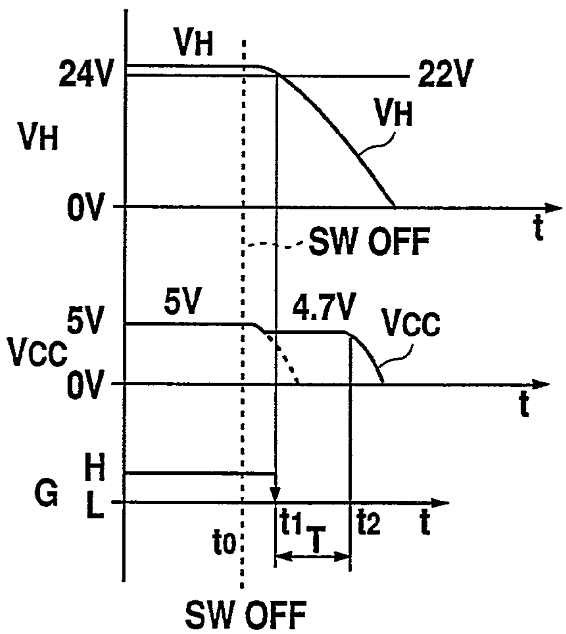

VH
24V
22V
VH
VH
0V
t
SW OFF
5V
4.7V
5V
VCC
VCC
0V
t
H
G
L
t1
T
t2
t
t0
SW OFF

Fig. 10

"A CONTROL INFORMATION STORAGE UNIT IN AN ELECTRONIC INSTRUMENT"

The present invention relates to a control information storage unit in an electronic instrument and, more particularly, to an improved control information storage unit for storing control information which is necessary for the guaranteed operation of an electronic instrument and which is preset or changed, if necessary, and for maintaining the control information even when the power source of the electronic instrument is off.

In a peripheral electronic instrument in a computer such as a printer, various kinds of control data are preset or changed as desired so as to provide desired control data concerning the operation of the electronic instrument. Such control data are different in electronic instruments. For example, a printer generally requires the control information on: the amount of correction of the position of paper at the time of autoloading; the length of the ink ribbon continuously used, which is necessary for indicating when to replace the ink ribbon; the cumulative operating time, which is necessary for indicating when the printer

needs inspecting; the frequency of use of each printing wire; whether or not an autoloading mechanism is mounted on the printer; and the selected font.

Such control information is set every time an electronic instrument such as a printer is used or changed during use. Conventionally, such control data are altered by switching a DIP switch or the like. However, an apparatus for storing control information in a RAM or the like provided in a controller without using such a DIP switch has recently been produced. This apparatus is advantageous in that a large amount of control information can be stored by a simple operation in comparison with a conventional DIP switch.

Such a RAM memory is a volatile memory, and since each of the preset data must be kept for a long time, the data must be maintained by a backup power source when the main power source of an electronic instrument is turned off. Such conventional RAM data are therefore backed up by a battery so that as soon as the power source is turned on, the control information necessary for the electronic instrument is taken out.

Such a backup equipment, however, involves the risk of losing the control information when the battery has run down. In addition, it is necessary to add a circuit structure for maintaining the voltage of the backup battery constantly at not less than a predetermined value.

Accordingly, it is an object of the present invention to eliminate the above-described problems in the related art and to provide an improved control information storage unit which stores control information in a volatile memory such as a RAM and constantly provides necessary control information during the operation of an electronic instrument, and which enables the control information to be stored reliably and confidently without the need for a backup battery when the power source is turned off.

To achieve this aim, in a control information storage unit according to the present invention, even a large amount of control information is stored in a reloadable volatile memory so as to be freely used during the operation of an electronic instrument in the same way as in the related art.

The characteristic feature of the present invention lies in the fact that an electrically reloadable nonvolatile memory such as an EEPROM is provided separately from the volatile memory such as a RAM, so that the control information stored in the volatile memory is written and stored in the nonvolatile memory when the power source of the electronic instrument is off. For this purpose, the control information storage unit according to the present invention is provided with a memory circuit for storing the control memory stored in the volatile memory in the

nonvolatile memory when the power source of the electronic instrument is turned off and the voltage is dropping.

According to the present invention, during the ordinary operation of an electronic instrument, the desired operation of the electronic instrument is carried out by using the control information stored in the volatile memory. At this time, the volatile memory maintains a voltage necessary for maintaining the data from the supply voltage which is in operation.

When the power source of the electronic instrument is turned off, the memory circuit reads out the control information which is written in the volatile memory in a very short time when the voltage is dropping and the read-out memory content is transferred to the nonvolatile memory such as an EEPROM.

Therefore, although the control memory in the volatile memory is erased when the power source is turned off, since the contents of the volatile memory are transferred to the nonvolatile memory such as an EEPROM, it is possible to maintain the control information for a long time without the need for a backup battery.

When the power source of the electronic instrument is turned on, the control memory is first written from the nonvolatile memory to the volatile memory such as a RAM, and

thereafter the operation of the electronic instrument is started.

According to the present invention, various conditions for the ordinary operation are set by using a volatile memory which has a high response speed and is capable of freely reading and writing, while the contents of the volatile memory are safely kept in a nonvolatile memory when the power source is turned off. It is therefore possible to provide a control information storage unit which is excellent both in operability and in the reliability of maintaining data.

The above and other objects, features and advantages of the present invention will become clear from the following description of the preferred embodiments thereof, taken in conjunction with the accompanying drawings.

Fig. 1 is a circuit diagram of a first embodiment of a control information storage unit according to the present invention which is applied to a printer;

Fig. 2 is an explanatory view of the operation of the first embodiment shown in Fig. 1;

Fig. 3 is a flowchart of the control information transfer operation in the embodiment shown in Fig. 1;

Fig. 4 is a flowchart of the reloading operation of the first embodiment shown in Fig. 1 while the power source is on;

Fig. 5 is a circuit diagram of a second embodiment of a control information storage unit according to the present invention which is applied to a printer;

Fig. 6 is a circuit diagram of a third embodiment of a control information storage unit according to the present invention which is applied to a printer;

Fig. 7 shows the wave form of the operation of the third embodiment shown in Fig. 6;

Fig. 8 shows the structure of the power circuit of a fourth embodiment of a control information storage unit according to the present invention which is applied to a printer;

Fig. 9 shows the entire structure and the voltage detector of the fourth embodiment shown in Fig. 8; and

Fig. 10 is an explanatory view of the operation of the fourth embodiment shown in Fig. 8.

The preferred embodiments of the present invention will be explained hereinunder with reference to the accompanying drawings.

Fig. 1 shows a first embodiment of a control information storage unit according to the present invention which is applied to a printer. As is known, the printer is composed of a printing mechanism 10 and a control board 11 including a control circuit. In this embodiment, an

operating voltage V_H of 24 V and a control voltage V_{CC} of 5 V are supplied to the printing mechanism 10 and the control board 11, respectively, from a power circuit 12. The printing mechanism 10 generally includes a paper feed mechanism, a carriage feed mechanism and a printing head, and the control board 11 includes a CPU 13 for controlling each element in accordance with a predetermined program. The CPU 13 is connected to a ROM 15, a RAM 16 and an EEPROM 17 through data buses 14. In this embodiment, the RAM 16 constitutes a volatile memory for storing various kinds of control data, while the EEPROM 17 constitutes a nonvolatile memory. According to this embodiment, the RAM 16 therefore supplies predetermined control information to the CPU 13 while the power source of the printer is on, and when the power source of the printer is turned off, the control information stored in the RAM 16 is transferred to the EEPROM 17.

The CPU 13 is in charge of the operation of transferring data from the RAM 16 to the EEPROM 17.

In Fig. 1, a voltage detector 18 is provided for detecting the off-operation of the power source of the power circuit 12. The voltage detector 18 outputs a detection signal G when the operating voltage V_H has dropped from 24 V, which is a normal voltage, to about 22 V, for example, and the CPU 13 executes the later-described interrupt

routine for data transfer in accordance with the detection signal G.

Fig. 2 shows the timing for data transfer when the power source of the printer is turned off in the first embodiment. When a power switch 12a is turned off (t_0) in Fig. 1, the voltage detector 18 observes that the operating voltage V_H drops to a reference voltage V_S, and outputs the detection signal G at the time t_1. The CPU 13 transfers the control information stored in the RAM 16 to the EEPROM 17 in accordance with the interrupt routine during the period of T, that is, between the time t_1 when the detection signal G is output and the time t_2 when the control voltage V_{CC} drops to a predetermined voltage.

Owing to the transfer of the control information, the data are safely kept in the nonvolatile memory, namely, EEPROM 17 even though the contents of the RAM 16 are lost when the power source is turned off.

Fig. 3 shows the transfer operation. When the interrupt routine is started in accordance with the detection signal G (step 100), the contents of the EEPROM 17 are first erased (step 101), and the control information stored in the RAM 16 is written into the EEPROM 17 (step 102). The writing operation is then verified (step 103). If the completion of the writing operation is confirmed (step 104), the process is finished. On the other hand, if

the writing operation is not yet completed at step 104, the process is returned to step 101, and the operations between step 101 and 103 are repeated. The transfer time is generally about between 10 and 50 msec, which is short enough to enable the data to be secured while the voltage is dropping due to the off operation of the power switch 12a.

Fig. 4 shows the operation of writing the control information stored in the EEPROM 17 into the RAM 16 when the power source is turned on. When the power source is turned on (step 200), all locations within the RAM 16 are cleared (step 201), and the data stored in the EEPROM 17 are written into the RAM 16 (step 202).

As described above, according to the present invention, while the power source of an electronic instrument such as a printer is on, a reloadable volatile memory such as a RAM stores control information and the electronic instrument can read out or write control information at such a high speed which enables the processing of even a large amount of control information at a highly responsive rate.

When the power source is turned off, the control information stored in the RAM is transferred to a nonvolatile memory such as an EEPROM while the voltage is dropping. It is therefore possible to maintain the control information in a stable state for a long time without the need for a backup voltage even while the power source is turned off.

As is well known, a nonvolatile memory such as an EEPROM is reloadable but the endurance limit is between 100,000 and 1,000,000 times. This endurance limit makes it impossible to use the nonvolatile memory for writing control information in a normal control information writing state unlike a RAM which enables free reloading. However, the nonvolatile memory is sufficiently usable if it is only used when the power source of the electronic instrument is turned on or off. Especially, in the case of recording control information for maintenance, it is necessary to accumulate control information for each operation of the printer. In this case, it is impossible to use a nonvolatile memory such as an EEPROM, but this embodiment, which uses a volatile memory for the ordinary storage of the control information, is free from such an inconvenience.

In the general case of reloading a nonvolatile memory, it is necessary to erase the information stored in the nonvolatile memory for each appropriate region before reloading, which means that the reloading operation takes a longer time than the operation of reloading a RAM or the like. In this embodiment, however, such a reloading operation is limited to the time when the power source is turned off, thereby enabling optimum control information storage due to the proper use of the relative merits of the volatile memory and the nonvolatile memory.

Fig. 5 shows a second embodiment of the present invention which is applied to a printer. This embodiment is similar to the first embodiment except for a slight difference in the circuit structure.

In the power circuit, a commercial voltage is supplied from a commercial power source plug 20 to a primary circuit 22 through a power switch 21, and an operating voltage V_H of 24 V is obtained through a transformer 24, a rectifying and smoothing circuit 25 and a stabilizer 26. The power circuit further includes a regulator 27 which outputs a control voltage V_{CC} of 5 V. The operating voltage V_H of 24 V is supplied to a printing head or a paper feeding motor in a printing mechanism in the same way as in the first embodiment, and the control voltage V_{CC} of 5 V is supplied to a control board in the same way as in the first embodiment. A voltage detector 28 generates a voltage V_L by the use of voltage-dividing resistors R_1 and R_2. The thus-obtained voltage V_L is compared with the reference voltage V_t by a comparator 30, and the result of the comparison is output as the detection signal G. Accordingly, in the second embodiment, the resistances of the resistors R_1, R_2 and the reference voltage V_t are set so that the detection signal G is output from the voltage detector 28 when the voltage V_H has dropped to a predetermined voltage, e.g., 22 V.

Fig. 6 shows a third embodiment of the present invention. The circuit structure for obtaining the detection signal G is shown. In Fig. 6, the control voltage V_{CC} of 5 V is obtained from a rectifying and smoothing circuit 31 and a stabilizer 32. The third embodiment is characterized in that a voltage outputting circuit for outputting a voltage V_R of +2 V having a small time constant is provided separately from a voltage circuit for outputting the control voltage V_{CC} of 5 V. For this purpose, an auxiliary secondary coil 33 is provided, and the voltage V_R of 2 V is constantly supplied to a comparator 36 by a diode 34 and a capacitor 35. The reference voltage V_S is supplied to the other input terminal of the comparator 36 by a Zener diode 37. A resistor 38 is connected in parallel to the capacitor 35 of the voltage output circuit so that the charged voltage of the capacitor 35 is rapidly discharged when the power source is turned off. The time constant at this time is set at a very small value.

According to this structure, immediately after the power switch 21 is turned off, the voltage V_R of 2 V of the voltage output circuit is discharged, and when the discharged voltage becomes lower than the reference voltage V_S, the detection signal G is output at the time t_1, as shown in Fig. 7. On the other hand, since the control voltage V_{CC} has a much larger time constant than the voltage output from

the voltage output circuit, the operation of transferring the control information stored in the RAM to the EEPROM is possible during the period in which a logic IC circuit is operational, that is, during the delay time T between the time t_1 when the detection signal G is output and the time t_2 when the control voltage V_{CC} drops to about 4.75 V.

Fig. 8 shows a fourth embodiment of the present invention. This embodiment is characterized in that not only are the operating voltage V_H of 24 V and the control voltage V_{CC} of 5 V generated from the power source but also an auxiliary voltage of 4.7 V is supplied from the voltage circuit for outputting the operating voltage V_H of 24 V to the voltage circuit for outputting the control voltage V_{CC} of 5 V so as to prevent the control voltage V_{CC} of 5 V from rapidly dropping when the power source is turned off.

In Fig. 8, the voltage supplied from the commercial power source through a plug 40 and a power switch 41 is dropped by a transformer 42, and is taken out of rectifiers 43, 44 as the operating voltage V_H of 24 V and the control voltage V_{CC} of 5 V, respectively. This embodiment is characterized in that a regulator 45 is provided in the voltage circuit for outputting the operating voltage V_H of 24 V. The regulator 45 supplies the auxiliary voltage of 4.7 V through a diode 46 to the voltage circuit for outputting the control voltage V_{CC} of 5 V.

According to this structure, even if the control voltage V_{CC} rapidly drops at the time t_0 when the power switch 41 is turned off, the output of the regulator 45 is maintained at 4.7 V for a sufficiently longer time. It is therefore possible to secure the transfer time T after the detection signal G is output.

Fig. 9 shows a voltage detector in the fourth embodiment. As is clear from Fig. 9, the operating voltage V_H of 24 V is not only supplied to the printing mechanism but also grounded through a Zener diode 47 and a resistor 48, thereby supplying an on-operation voltage to a transistor 49. To the collector of the transistor 49 are connected a voltage circuit for outputting the control voltage V_{CC} of 5 V and the base of a transistor 50. The collector of the transistor 50 is connected to the voltage circuit for outputting the control voltage V_{CC} of 5 V, and outputs the detection signal G as an interrupt signal to an NMI (non-maskable interrupt) input terminal of the CPU 13.

According to this structure, in the ordinary state in which the power source is on, the transistors 49 and 50 maintain the off state, and "H" is supplied to the NMI input terminal as the detection signal G.

When the power source is turned off and the operating voltage V_H has drops, the transistor 49 is turned off while the transistor 50 is turned on, so that "L" is output

as the detection signal G. The CPU 13 then starts the interrupt routine so as to transfer the control information stored in the RAM 16 to the EEPROM 17.

As is clear from Fig. 10, according to this embodiment, the control voltage V_{CC} of 5 V rapidly drops as indicated by the broken line when the power source is turned off. By supplementing the dropping voltage by a voltage from the voltage circuit for outputting the operating voltage V_H of 24 V, it is possible to maintain a voltage of 4.7 V for the predetermined time T necessary for transferring the control information.

As described above, according to the present invention, various kinds of control data necessary for a peripheral electronic instrument used with a computer, such as a printer, are stored in a volatile memory, such as a RAM, during the on state of the power source, while the control information is stored in a nonvolatile memory, such as an EEPROM, when the power source is turned off. The control information storage unit in an electronic instrument according to the present invention is therefore advantageous in that it is possible to maintain a large amount of control information securely and safely without the need for a backup power source.

While there has been described what are at present considered to be preferred embodiments of the invention, it will be understood that various modifications may be made

thereto, and it is intended that the appended claims cover all such modifications as fall within the true spirit and scope of the invention.

CLAIMS:

1. A control information storage unit in an electronic instrument comprising:

(a) a power circuit for supplying a predetermined voltage to said electronic instrument;

(b) a voltage detector for detecting the off-operation of a power source and outputting a detection signal when the voltage output from said power circuit has dropped;

(c) a volatile memory for storing operation control information for said electronic instrument;

(d) a nonvolatile memory for storing said operation control information for said electronic instrument when said power source is turned off; and

(e) a memory control circuit for receiving said detection signal supplied from said voltage detector and storing said control information stored in said volatile memory in said nonvolatile memory at the time that said detection signal is received.

2. A control information storage unit in an electronic instrument according to Claim 1, wherein

said predetermined voltage in said power circuit (a) includes an operating voltage and a control voltage;

said voltage detector (b) includes:

two voltage-dividing resistors for generating a low voltage from said operating voltage;

a Zener diode for producing a reference voltage;

a comparator for comparing said low voltage with said reference voltage; and

a means for outputting said detection signal when said low voltage has become lower than said reference voltage; and

said memory circuit (e) stores said control information stored in said volatile memory in said nonvolatile memory during the period between the time when said detection signal is received and the time when said control voltage drops to a predetermined voltage.

3. A control information storage unit in an electronic instrument according to Claim 1, wherein

said predetermined voltage in said power circuit (a) is a control voltage;

said power circuit (a) includes:

(f) a voltage output circuit for generating a voltage having a smaller time constant than said control voltage,

said voltage output circuit including a diode and a capacitor for producing said voltage having said small time constant, and a resistor connected in parallel to said capacitor so as to discharge said voltage having said small time constant when said power source is turned off;

said voltage detector (b) includes:

a Zener diode for producing a reference voltage;

a comparator for comparing said voltage discharged from said voltage output circuit when said power source is turned off with said reference voltage; and

a means for outputting said detection signal when said discharged voltage has become lower than said reference voltage; and

said memory circuit (e) transfers said control information stored in said volatile memory to said nonvolatile memory during the delay period between the time when said detection signal is received and the time when said control voltage drops to a predetermined voltage.

4. A control information storage unit in an electronic instrument according to Claim 1, wherein

said predetermined voltage in said power circuit (a) includes an operating voltage and a control voltage;

said voltage detector (b) includes:

(g) two rectifiers for taking out said operating voltage and said control voltage separately from each other;

(h) a regulator provided in the circuit for outputting said operating voltage; and

(i) a means for supplying an auxiliary voltage from said regulator to said circuit for outputting said control voltage; and

said memory control circuit (e) stores said control information stored in said volatile memory in said

nonvolatile memory during the period between the time when said detection signal is received and the time when said auxiliary voltage supplied to said control voltage drops to a predetermined voltage.

5. A control information storage unit in an electronic instrument according to Claim 1, wherein

said predetermined voltage in said power circuit (a) includes an operating voltage and a control voltage;

said power circuit (a) includes:

a first transistor for outputting an on-operation voltage to said operating voltage;

a second transistor connected to said control voltage on the collector side of said first transistor; and

a means for outputting "H" as said detection signal when said power source is turned off, said operating voltage drops to a predetermined voltage, said first transistor is turned off and said second transistor is turned on; and

said memory circuit (e) is connected to said circuit for outputting said control voltage and has an interrupt terminal for receiving said detection signal from said collector of said second transistor, said memory contol circuit (e) executing an interrupt program routine for transferring said control information in said volatile memory to said nonvolatile memory to be stored during the period from the reception of said detection signal by said

interrupt terminal to the dropping of said control voltage to a predetermined voltage, therby generating an interrupt.

6. A control information storage unit in an electronic instrument according to Claim 1, wherein said nonvolatile memory is an EEPROM.

7. A control information storage unit in an electronic instrument according to Claim 2, wherein said nonvolatile memory is an EEPROM.

8. A control information storage unit in an electronic instrument according to Claim 3, wherein said nonvolatile memory is an EEPROM.

9. A control information storage unit in an electronic instrument according to Claim 4, wherein said nonvolatile memory is an EEPROM.

10. A control information storage unit in an electronic instrument according to Claim 5, wherein said nonvolatile memory is an EEPROM.

11. A method of storing control information for an electronic instrument comprising the steps of:

(a) detecting the off-operation of the power source of a voltage detector by a change in the operating voltage and the control voltage supplied from a power circuit;

(b) outputting a detection signal from said voltage detector to a memory circuit;

(c) erasing the contents of a nonvolatile memory and writing the control information stored in a volatile memory in said nonvolatile memory;

(d) clearing all the contents of said volatile memory when said power source is turned on; and

(e) writing the data stored in said nonvolatile memory in said volatile memory.

12 A method of storing control information for an electronic instrument according to Claim 11 wherein

said step (b) is executed when said operating voltage supplied from said power circuit drops; and

said step (c) is executed during a predetermined time between the time when said detection signal is output and the time when said control voltage drops to a predetermined voltage.

13. A method of storing control information for an electronic instrument according to Claim 11, wherein said nonvolatile memory is an EEPROM.

14. A method of storing control information for an electronic instrument according to Claim 12, wherein said nonvolatile memory is an EEPROM.

15. A control information storage unit substantially as hereinbefore disclosed with reference to and as shown in any of the accompanying drawings.

16. A method of storing control information substantially as hereinbefore disclosed with reference to and as shown in any of the accompanying drawings.

- 23 -

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number
GB 9212854.5

Relevant Technical fields

(i) UK Cl (Edition K) G4A (AEP)

(ii) Int Cl (Edition 5) G06F 12/16, 11/00

Search Examiner
S J PROBERT

Databases (see over)
(i) UK Patent Office

(ii) ONLINE DATABASE: WPI

Date of Search
2 SEPTEMBER 1992

Documents considered relevant following a search in respect of claims 1 TO 16

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	GB 2201268 A (MOTOROLA) see whole document	1-16
X	US 4327410 (PATEL et al) see whole document, particularly column 1 line 50 to column 2 line 5	1-16

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

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Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

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